Claims

We claim:

1. A capacitive isolation system for providing a digital communication channel across one or more isolation capacitors between a data input terminal and a data output terminal, the isolation system comprising:

an encoder circuit connected to receive digital data input signals from the input terminal, the encoder circuit including logic circuitry for combining the data input signals with control signals, the encoder circuit providing a digital encoded signal at an encoder output;

a driver circuit connected to the encoder output and to a first side of the isolation capacitors, the driver circuit adapted to receive the encoded signal and to apply it to the first side of the isolation capacitors;

a clock recovery circuit connected to the second side of the isolation capacitors to receive an isolated encoded signal therefrom, the clock recovery circuit providing a clock signal synchronized with the isolated encoded signal on the second side of the isolation capacitors;

a data latch connected to the second side of the isolation capacitors and to the clock signal, the data latch comprising a clocked latch circuit and adapted to provide a synchronized encoded data signal synchronized with the clock signal; and

a decoder circuit connected to receive (a) the synchronized encoded data signal from the data latch and (b) the clock signal, the decoder circuit adapted to separate the synchronized encoded data signal into control signals and isolated digital data signals, the isolated digital data signals being presented at the output terminal of the system.

2. The system of claim 1, wherein the driver circuit is a differential driver circuit.

3. The system of claim 1, further comprising an isolated power supply circuit connected to the second side of the isolation capacitors, the power supply circuit including a rectifier circuit for converting a portion of the energy in the synchronized encoded data signal into a DC voltage signal that is connected to provide DC power to other isolated circuitry.

4. The system of claim 3, wherein the DC voltage signal is connected to provide power to the clock recovery circuit.

5. The system of claim 3, wherein the DC voltage signal is connected to provide power to the decoder circuit.

6. The system of claim 1, further comprising an analog-to-digital converter connected to the input node.

7. The system of claim 1, further comprising a digital-to-analog converter connected to the output node.

8. The system of claim 1, wherein the clock recovery circuit comprises a phase-locked-loop circuit and a filter circuit.

9. A bidirectional isolation system for providing an isolated communication channel for digital signals in a forward direction and in a reverse direction across a capacitive isolation barrier, the system comprising:

an isolation barrier comprising one or more capacitors;

a powered system on a first side of the isolation barrier, the powered system comprising:

a powered driver circuit connected to at least one of the capacitors for driving a forward direction signal across the isolation barrier,

a powered encoder circuit having an input terminal for receiving a digital signal to be transmitted in the forward direction across the barrier and having an output connected to the powered driver circuit, and

a powered decoder circuit having an input connected to at least one of the capacitors, the powered decoder circuit adapted for receiving and decoding signals transmitted in the reverse direction across the isolation barrier; and

an isolated system on a second side of the isolation barrier, the isolated system comprising:

a clock recovery circuit having an input connected to at least one of the barrier capacitors and an output providing an isolated clock signal to circuitry in the isolated system;

an isolated decoder circuit connected to at least one of the capacitors and providing a decoded digital data signal;

an isolated driver circuit connected to at least one of the capacitors for driving signals in the reverse direction across the isolation barrier; and

an isolated encoder circuit having an input for receiving a digital signal to be transmitted in the reverse direction across the barrier and having an output connected to the isolated driver circuit.

10. The system of claim 9, the isolated system further comprising an isolated power supply circuit connected to at least one of the isolation capacitors, the power supply circuit including a rectifier circuit for converting a portion of the energy in the data signal into a DC voltage signal that is connected to provide DC power to other circuitry in the isolated system.

11. The system of claim 9, further comprising a data latch connected to receive the forward direction signal and the clock signal and having an output providing a synchronized data signal to the isolated decoder circuit.

12. An isolation system for transmitting a digital data signal across a capacitive isolation barrier, comprising:

one or more isolation capacitors;

means for providing a digital signal to a first side of the capacitive isolation barrier;

means for receiving a corresponding isolated signal from a second side of the isolation barrier;

clock recovery means for recovering a clock signal from the isolated signal; and

means for synchronizing the isolated signal with the clock signal.

13. The system of claim 12, further comprising means for generating a DC voltage from the isolated signal for use in powering said clock recovery means.

14. The system of claim 12, further comprising encoder means for combining said digital signal with control information to be transmitted across the isolation barrier, and decoder means for separating the digital data signal from the isolated signal.

15. A method of transmitting a digital data signal across a capacitive isolation barrier, comprising:

combining the digital data signal with control information to form a digital encoded signal;

driving the digital encoded signal across the capacitive isolation barrier;

receiving an isolated encoded signal from the isolation barrier;

recovering a clock signal from the isolated encoded signal;

synchronizing the isolated encoded signal with the clock signal; and

separating the isolated encoded signal into an isolated digital data signal and isolated control information.

16. The method of claim 15, further comprising generating a DC power supply signal from the isolated encoded signal.

17. An isolation system for providing a digital communication channel between a powered circuit and an isolated circuit, the isolation system comprising: an isolation barrier and a clock recovery circuit located on an isolated side of the isolation barrier, the clock recovery circuit adapted to provide a recovered clock signal based on isolated signals received from the powered circuit across the isolation barrier, the recovered clock signal being that is substantially free of phase noise.

18. The isolation system of claim 17, wherein the isolation barrier comprises one or more capacitors.

19. The isolation system of claim 17, wherein the digital communication channel is bidirectional.

20. The isolation system of claim 17, wherein the clock recovery circuit comprises a phase-locked loop circuit.

21. The isolation system of claim 20, wherein the phase-locked loop circuit comprises a loop filter circuit for reducing the effects of phase noise on the recovered clock signal.

22. The isolation system of claim 17, wherein the isolated signals are data signals.

23. The isolation system of claim 17, wherein the isolated signals are clock signals.

24. A bidirectional isolation system for providing an isolated communication channel for data signals in a forward direction and in a reverse direction across an isolation barrier comprised of isolation elements, the system comprising:

(a) a powered system on a first side of the isolation barrier, the powered system comprising a first driver circuit connected to the isolation barrier for driving a forward direction digital signal across the isolation barrier; and

(b) an isolated system on a second side of the isolation barrier, the isolated system comprising an second driver circuit connected to the isolation barrier for driving a reverse direction digital signal across the isolation barrier;

wherein the forward direction digital signal and the reverse direction digital signal are both driven through the same isolation elements.

25. The isolation system of claim 24, wherein the isolation elements are capacitors.

26. The isolation system of claim 24, wherein the first and second driver circuits are differential driver circuits.

27. The isolation system of claim 24, wherein the forward direction digital signal comprises said data signal multiplexed with a control signal.

28. The isolation system of claim 24, wherein the forward direction digital signal comprises said data signal multiplexed with a control signal.

29. An isolation system for providing a digital communication channel for data signals and control signals, the isolation system comprising:

an isolation barrier;

a multiplexer located on one side of the isolation barrier and connected to receive the data signals and the control signals and providing a multiplexed digital signal that is connected to the isolation barrier;

a demultiplexer located on the other side of the isolation barrier and connected to receive the multiplexed digital signal from the isolation barrier, the demultiplexer having a data signal output and a control signal output.

30. The system of claim 29, wherein the isolation barrier is a capacitive isolation barrier.

31. The system of claim 29, wherein the multiplexed digital signal is conveyed across the isolation barrier as a differential digital signal.

32. The system of claim 29, further comprising

a second multiplexer located on said other side of the isolation barrier and connected to receive the data signals and the control signals and providing a multiplexed digital signal that is connected to the isolation barrier;

a second demultiplexer located on said one side of the isolation barrier and connected to receive the multiplexed digital signal from the isolation barrier, the demultiplexer having a data signal output and a control signal output;

whereby bidirectional multiplexed communication of data and control signals across the isolation barrier is enabled.